2838

TRANSMITTAL LETTER (General - Patent Pending)

Docket No. P 7675.10005

In Re Application Of: Ionel Jitaru

MAR 20 2003

TECHNOLOGY CENTER 2800

Serial No. 09/260,478

Filing Date March 1, 1999 Examiner

Group Art Unit

Gary L. Laxton

2838

Title:

SOFT TRANSITION CONVERTER

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UNITED STATES PATENT AND TRADEMARK OFFICE

Response 2.016 3-21-03

PATENT EXAMINING OPERATIONS

MAR 20 2003

TECHNOLOGY CENTER 2800

Applicant:

Ionel Jitaru

Group Art Unit:

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Serial No.:

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Examiner:

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SOFT TRANSITION CONVERTER

CERTIFICATE OF FIRST CLASS MAILING

(37 CFR 1.8)

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 6TH day of March, 2003.

I H Rouske

Birdwell, Janke & Durando, PLC 1100 SW Sixth Avenue, Suite 1400 Portland, OR 97204

March 6, 2003

RESPONSE

Box: Fee Response Commissioner for Patents Washington DC 20231

Greetings:

This is in response to the Office Action mailed November 6, 2002.

Section 103 Rejections

Claims 1 and 4 - 6 stand rejected under 35 USC §103 as being unpatentable over

Okamoto, U.S. Patent No. 4,564,897 ("Okamoto") in combination with Morris, U.S. Patent No.

5,555,494 ("Morris"). The Office Action alleges that Okamoto discloses all that is claimed except the claimed dead time, and that Morris teaches use of a dead time to "provide an efficient

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converter circuit." Applicant respectfully traverses the rejections, because the assertion that Morris teaches the use of a dead time in any power converter to increase efficiency is incorrect.

Morris explains that the dead time is *necessary* in certain types of converters, (Col. 10, lines 29 - 28). The reason for this can be seen by considering the primary circuit of Morris. Morris uses a DC source and primary switching transistors to convert the DC to AC. The dead time is used as a safety margin to prevent cross-conduction in the primary switching transistors, which would short circuit the source. Specifically, switches SW1 and SW4 are "on" while switches SW2 and SW3 are "off" and vice versa. If SW1 and SW4 are turned "on" at the very same time that SW2 and SW3 are turned "off", there is the possibility, for a limited time, of the existence of a short circuit through SW1 and SW3, and/or through SW2 and SW4. The dead time provides a safety margin that prevents this short circuit condition from occurring. It can be readily appreciated that the dead time actually *decreases* efficiency because, during the dead time, no power can be produced by the converter. Accordingly, Morris <u>does not</u> assert that it is *desirable* to employ a dead time to increase efficiency.

By contrast with Morris, Okamoto already has an AC source, and does not need or employ any primary switching transistors. Therefore, Okamoto does not exhibit the problem that Morris uses the dead time to solve, and there is no reason to produce a dead time in Okamoto based on any teaching of Morris.

For these reasons, it is respectfully submitted that the allegation that it would have been obvious to modify Okamoto based on the teachings of Morris is incorrect, the claims are

patentable over the references of record, and the examiner is respectfully requested to allow claims 1 - 7 and pass this case to issue.

Respectfully submitted,

Garth Janke

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